IEEE MELECON 2004, May 12-15, 2004, Dubrovnik, Croatia

Constraint Driven Dual-rail PLA Module Generator with Embedded 2-Input Logic Cells

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***Abstract*—This paper describes design and development of a module generator which is based on a timing-driven design methodology. This generator uses a design constraint to achieve a flexible transistor sizing in a logic cell generation part. In addition, generated logic cells can be easily adapted to a layout generator. Almost all of these logic cells have two inputs. 2-input logic cells are embedded in place of conventional AND/OR planes. By using the 2-input logic cells, some classes of logic functions can be implemented in a smaller circuit area. Moreover, an HDL model generator is developed to create delay behavior models easily and quickly with precise timing parameters.**

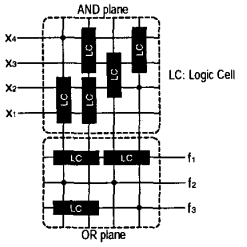

Fig. 1. PLA structure for generation

I. Introduction

Since their introduction in 1970, programmable logic arrays have been used in large-scale integration chips, due to PLAs' providing regularity, programmability and flexibility. Recently, PLAs have experienced a renewed interest as a logic implementation style for high-performance design. The IBM 1 Gigahertz processors[1] utilized PLAs to implement control logic. The stated reasons of this choice were high speed and the ability to quickly implement.

The design methodology using PLAs does not require the iteration of the design process because the structured arrays give predictable area, delay, and power consumption early in design process, which is quite an attractive feature for the modern GHz circuits design [2], [3].

Design complexity of the VLSI systems is increasing with the increase of the circuit elements in a single chip. Therefore the design complexity is becoming one of the most important issues in circuit design. This paper demonstrates the development of a PLA module generator to overcome the design complexity as a plus to the PLA's regular structure. An automatic generation is necessary for efficient characterization, quick and unerring transistor layout and HDL model generation, so that the design complexity can be reduced partially and human errors minimized by automatic generation.

Section 2 presents the PLA structure which is used in generation. Section 3 introduces the proposed module generator and its specifications. Experimental results are given in section 4 with conclusions in section 5.

II. PLA Structure Used In Generation

Figure-1 shows the PLA structure. In addition to the conventional PLAs, this PLA utilizes optionally 2-input logic cells (LCs) in each of the planes [4]. Though it is illustrated as a single rail PLA, the present PLA is utilizing dual-rail inputs, $X_i$and $\overline{X_i}$. The 2-input logic cells can realize any 2-input Boolean function and are embedded in a dual-rail PLA. The 2-input logic cells can be realized by reconnecting some local wires, thus there is almost no effect on delay and area when it is compared with the conventional AND/OR cells. The number of product terms was reduced. Thus, the reduction of the number of product terms leads to the reduction of the area, so that high-speed and low power operation is achieved. Basic cells used in this generation are shown in Figure-2a. Figure-2b shows the logic cells which are realized by the basic cells.

Figure-4 shows the column circuit of PLA. It is based on a dual-rail bit-line and a latch sense amplifier. Output signals are obtained by sensing the differential voltage of the dual-rail bit-line. Logical OR and NOR of the functions of logic cells can be obtained from the output signals. The X_1 to X_n signals are the primary inputs or their negations. Virtual Ground, VG is provided to reduce the voltage swing of the bit-lines. The PC signals precharges and equalizes the bit-lines. $\overline{PC}$ discharges the $\overline{BL}$ every read-out cycle. The SAE signal activates and isolates the sense amplifier from the bit-lines in order to reduce the load capacitance. The purpose of the dummy transistor, whose the gate terminals are connected to ground, is to balance the load capacitance and the leakages current of bit lines.

The timing diagram of the control signals is shown in Figure-3. The column circuit operates in two phases. In phase-1, the PC signals, X_1 to X_n and their negations are low. Thus, the bit-lines are precharged high and equalized. At that time VG node is discharged to low. Phase-2 starts when the PC signal becomes high and the primary inputs are activated. In the phase-2, $\overline{BL}$ is pulled down by charge sharing with VG node through the reference cell every cycle. When at least one of the primary inputs is high and

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TABLE I

COMPARISON BETWEEN DIFFERENT IMPLEMENTATION STYLES

Circuit	# Product Terms	Area (μm^2)	Delay (ns)	Power Consumption (mW)	ADP Product (normalized)
Conventional single-rail PLA[6]	220	490,965	4.19	99	1.00
Conventional dual-rail PLA[7]	220	939,798	1.52	73	0.512
Proposed PLA	136	601,624	1.39	43	0.177

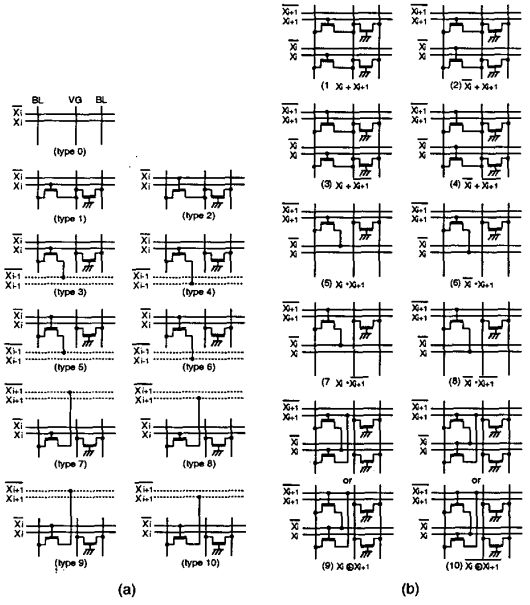

Fig. 2. (a) Basic cells (b)2-Input logic cells

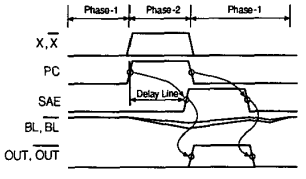

Fig. 3. Timing diagram

at least one of the logic cells pulls BL down, the voltage potential of BL becomes lower than the voltage potential of $\overline{BL}$. Otherwise BL stays high. In the case of one logic cell discharging, the discharge speed of BL is twice of the discharge speed of $\overline{BL}$. This is because the device size of the reference cell is 0.5W. This half-size device is provided to avoid the meta-stable condition, which may be caused when there is no pull-down path on BL. On the other hand, when all the primary inputs are low, BL stays high and $\overline{BL}$ is discharged through VG. The SAE signal is activated when the developed voltage difference between the bit-lines becomes larger than the designed sense voltage which takes the worst case of considerable noise margin and process variations into account. The performance comparison with the other implementation styles is shown in Table-1. The configuration of the PLA is shown in Figure-5. Dummy cells in the dummy column are designed in the minimum size in order to generate an enabling signal to the OR plane.

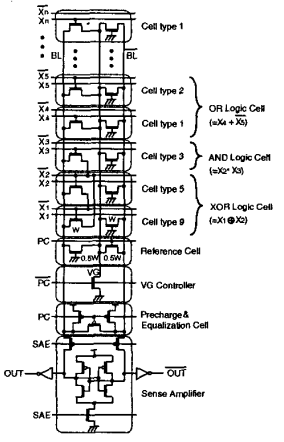

Fig. 4. Schematic of the column circuit

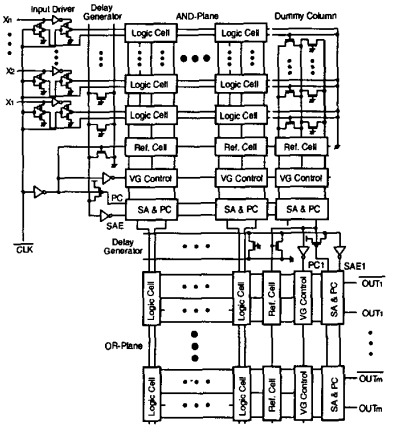

Fig. 5. PLA configuration

III. DESIGN METHOD OF PLA MODULE GENERATION

This PLA module generator needs desired target delay and a personality matrix as input data. Beside these inputs there is some other input data, such as design rules, physical layout parameters and transistor models, which are not entered from the generator screen but included while generation. Personality matrix includes the desired function to be implemented. Layout in GDS-II format and a timing annotated HDL behavior model are the outputs of the generator. This PLA module generator consists of five different parts; Logic Synthesis [5],Transistor Sizing and Logic Cell Generation, Layout Generation, Stimulus Generation, HDL Model Generation, respectively. Figure-6 shows the flow chart of the PLA module generation. In this paper, inparticularly we will focus on the last four modules.

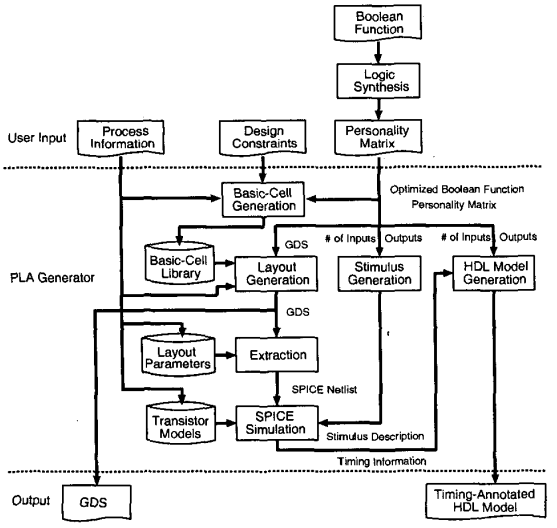

Fig. 6. Flow chart of PLA module generation

TABLE II

SYMBOLS AND CORRESPONDING BASIC CELLS OF PERSONALITY MATRIX

Symbol	Basic Cell Type
-	type 0
0	type 1
1	type 2
2	type 3
3	type 4
4	type 5
5	type 6
6	type 7
7	type 8
8	type 9
9	type 10

A. Logic Synthesis Method[5]

The purpose of logic synthesis is to minimize the number of product terms needed. The basic idea of synthesizer is, finding 2-input logic terms contained in a given Boolean function. Personality Matrix is obtained from the output of a logic synthesizer. We defined some symbols corresponding to basic cells which can be seen in Table-2. An example of personality matrix is shown in Figure-7.

B. Transistor Sizing, Logic Cell and Layout Generation

The logic cell generation module needs target delay and process information for deciding the transistor size of logic cells. The larger size of the logic cell transistors the smaller the circuit delay. This relation is shown in Figure-8. Delay is normalized by an inverter delay. 1 inverter delay is equal to about 100 ps for 0.35 um^2 process technology.

The layout generator needs process information and personality matrix as inputs. It has a two-step process. The first process is the generation of the circuit elements. Sense amplifier, precharge and equalization circuit, control signals generator, driver circuits (input, output, clock and control drivers), delay generator circuit, dummy cell of delay generator, reference cell, VG controller, dummy column

X1X2X3X4	Y1Y2
1 0 1 0 - 4 - 2 8 - 1 -	0 1 2 - - 4

Fig. 7. Example of personality matrix

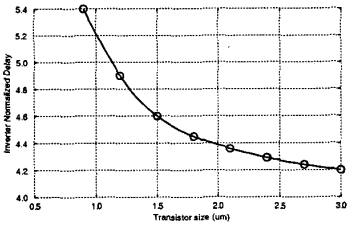

Fig. 8. Relationship between delay and transistor size

circuit, VDD and GND circuits are generated in the layout generation module. These elements can be seen in Figure-5. The dummy cell of the delay generator is designed in the minimum size. The number of delay generator dummy cells are decided according to the sense amplifier voltage which activates the outputs.

The second process step is the placement of the circuit elements. Personality matrix shows the circuit configuration. Placement will be done according to this configuration. Given design rules and the size information of the circuit elements are the two other important factors on placement. Due to the regular nature of the logic cells the complete generation process is automated with efficient space and time usage.

C. Stimulus Generation

Stimulus generation is one of the process steps, at which the shape of the input waves is designed. Three kinds of data are necessary for this step, input data, netlist data and technology model file. The input signals and the clock signal are generated in the stimulus module. SAE, PC and $\overline{PC}$ signals are generated from the clock signal then passed to the HSPICE simulation.

D. HDL Behavior Model Generation

Our final target is to create a Verilog HDL model code of a given boolean function. The HDL model generation module needs a personality matrix data and timing information. A timing-annotated HDL behavior model is the output of this module. HDL behavior model is generated by writing the logical expression of personality matrix. The longest path is detected and the logical expression of the longest path is generated for the maximum delay. The circuit delay described in an HDL behavior model shows the propagation delay of all the ouput signals. For the calculation of hold time, the output signal becomes high when the voltage difference between maximally loaded bit-lines becomes larger than a decided sense voltage. Thus inputs must be stable before that time. Set up time depends on the drive capability of the input drivers.

TABLE III
COMPARISON OF CIRCUIT DELAY AND CPU TIME

Circuit	Inputs	Product Terms	Logic Cells	Delay (ns)	CPU time (sec)
Example-1	16	87	621	1.01	33.1
Example-2	32	144	1459	1.25	117.8
Example-3	64	220	3368	1.39	441.2

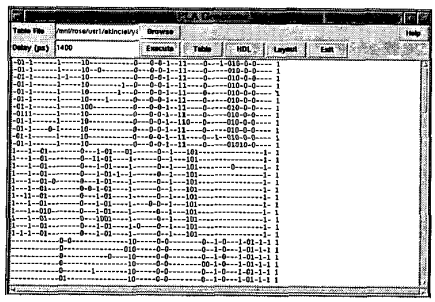

Fig. 9. PLA module generator

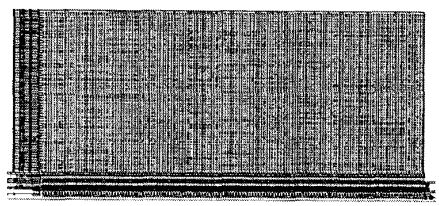

Fig. 10. Generated layout

IV. EXPERIMENTAL RESULTS

A PLA module generator with 2-input logic cells has been designed and implemented on UNIX system. It can be seen in Figure-9. "Table" and "Delay" are the inputs of module generator, and they are given by the user. The outputs can be seen from the lower window on the screen. Figure-10 shows a generated PLA layout in GDS-II form. Figure-11 shows a timing-annotated HDL behavior model of personality matrix in Figure-9. The necessary timing parameters such as delay, and hold time are taken from the simulation results.

This module generator was applied to some logic circuits. The circuits were designed using a 0.35 um, 3-metal-layer CMOS technology with a supply voltage of 3.3 V. Table-3 shows the circuit delay and CPU time of PLA generation in three different circuits. The results show that even the biggest circuit can be generated in 8 minutes. In addition, Figure-12 shows the comparison between standart cell based design and logic cell based PLA. The results show that logic cell based PLA requires on average 3.29 times the area of the standart based design. The reason of that ratio is dual-rail structure design. The delay of logic cell based PLA is 0.56 times on average. The reason of that ratio is high speed-capability of sense amplifier and 2-level logic implementation with 2-input logic cells.

V. CONCLUSION

A PLA module generator has been developed which combines the logic synthesis for the dual-rail PLA with

```
module pla(clk, x, f);
 input clk;
 input [3:0] x;
 output [1:0] f;
 reg[2:0] y;
 parameter delay = 0.93;
 always @(posedge clk) begin
  y[0] <= ~x[0] | x[1] | ~x[2] | x[3];
  y[1] <= x[0] & ~x[1] | ~x[2] & x[3];
  y[2] <= ~x[0] & x[1] | ~x[2];
 end
 specify
  $ setup (x, posedge clk, 0.10);
  $hold  (posedge clk, x, 0.17);
 endspecify
 assign #delay f[0] = y[0] | y[0] & y[1];
 assign #delay f[1] = ~y[0] | y[1] & ~y[2];
endmodule
```

Fig. 11. Generated HDL behavior model

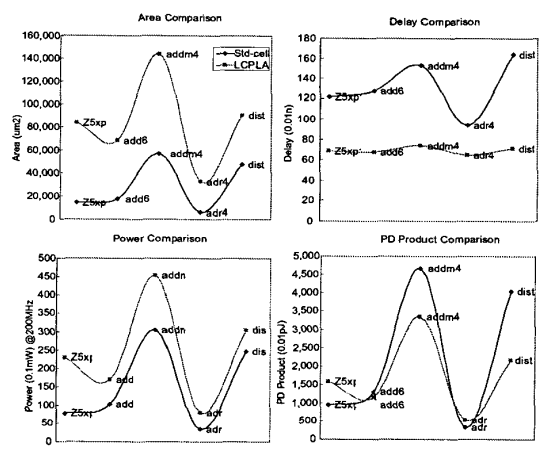

Fig. 12. Comparison of standard-cell based and logic-cell based design

embedded 2-input logic cells and its layout circuit design . The PLA module generator basicly has transistor sizing module, layout generator module and timing-annotated HDL behavior model module. A generated layout and a behavior model with 64-bit inputs and 220 product terms were obtained within 8 minutes on a Sun UltraSPARC-III 900 MHz processor.

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