A Dual-Rail PLA with 2-Input Logic Cells

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Abstract

This paper presents a new dual-rail PLA with 2-input logic cells. The 2-input logic cells composed of pass-transistors can realize any 2-input Boolean function and are embedded in a dual-rail PLA without degradation of circuit performance. By using the logic cells, some classes of logic function can be implemented in a smaller circuit area, so that a high-speed and low-power operation is also achieved. The area advantage over the conventional design has been demonstrated by using PLA benchmark circuits. The measured results show that the proposed PLA operates correctly.

1. Introduction

In the past three decades, *programmable logic arrays* (PLAs) have been widely used for combinational and sequential logic circuits because of its simplicity, regularity, and flexibility. These features are becoming more and more important in recent complicated VLSI systems, where regular structures and simple designs are required in order to shorten the design and test time. For example, control logics of the IBM 1-GHz 64-bit PowerPC processors, *Rivina* [1] and *guTS* [2], have been realized in PLAs to reduce the design complexity. The design methodology using PLAs does not require the iteration of the design process because the structured arrays give predictable area, delay, and power consumption early in the design process. In addition, the issues of signal integrity such as cross-talk, which are becoming increasingly important in deep sub-micron (DSM) IC designs, can be easily predicted and alleviated by taking advantage of the regularity of PLAs [3].

On the other hand, although the structural regularity of PLAs offers design simplicity, PLAs generally require a large chip area compared to random logic implementation. To overcome this drawback, some variant structures of PLA which implement Boolean functions efficiently have been proposed, such as a PLA with input decoders [4]. However, this structure degrades a circuit performance due to an additional gate delay of decoders.

In this paper, we propose a new dual-rail PLA with 2-input logic cells which can reduce the overall area of PLA. The 2-input logic cells composed of pass-transistors can realize any 2-input Boolean function and are embedded in a dual-rail PLA without degradation of circuit performance. By using the logic cells, some classes of logic function can be implemented in a smaller circuit area, so that a high-speed and low-power operation is also achieved.

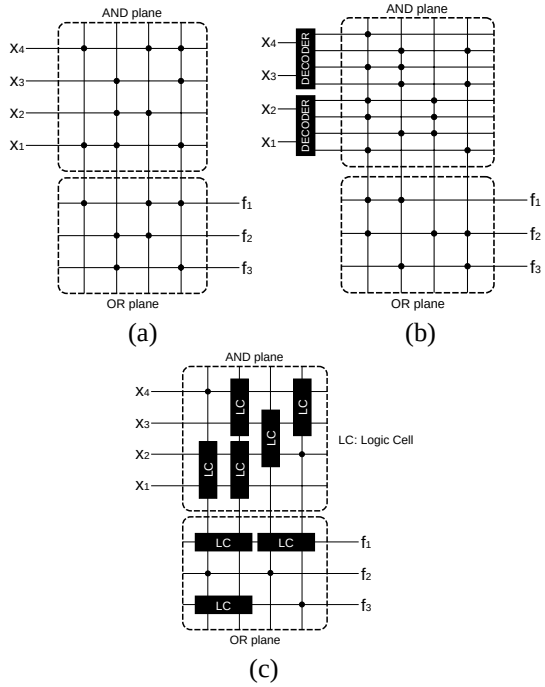

Figure 1. Structures of (a) the conventional PLAs (b) with input decoders and (c) the proposed PLA.

2. Conventional and Proposed PLA Structures

Figure 1(a) shows the structure of the conventional PLA which is widely used in VLSI systems [5]. The X_n and f_n signals are the primary input or its negation and the output of the PLA, respectively. It contains an AND-plane and an OR-plane, and is capable of implementing any Boolean function expressed in the sum-of-products form by connecting switching transistors, which are denoted by dots in the figure, to the input and output wires. In general, this PLA is, however, known as the structure which may not be suitable for designs that have inherent multi-level logic structures such as arithmetic circuits [6].

The PLA with input decoders shown in Figure 1(b) has been proposed to implement Boolean functions efficiently [4]. By using decoders, the number of product terms can be reduced, thus resulting in a smaller circuit area. However, this structure degrades the circuit performance due to an additional gate delay of decoders.

In contrast, the proposed PLA utilizes 2-input logic cells (LCs) in each of the planes as shown in Figure 1(c).

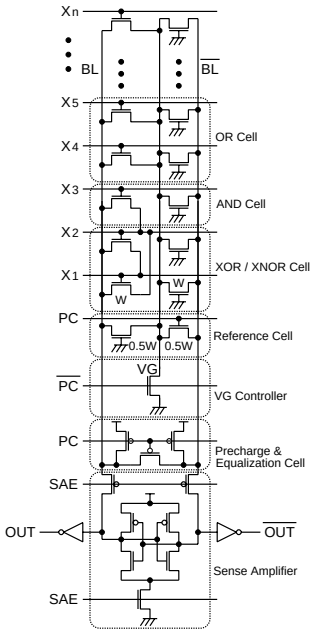

Figure 2. Basic circuit of the proposed PLA.

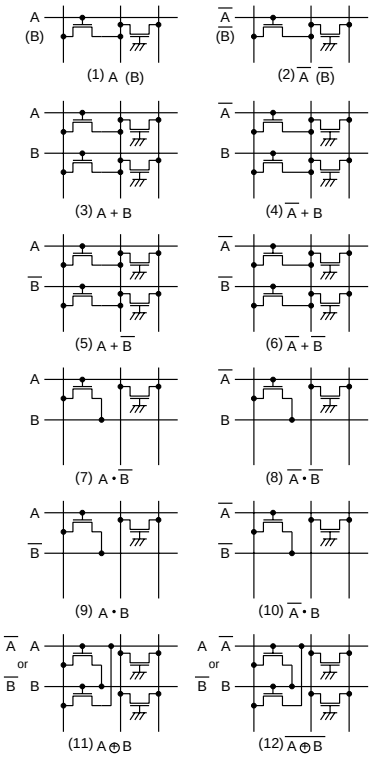

Figure 3. Logic cells (LCs) for the basic circuit.

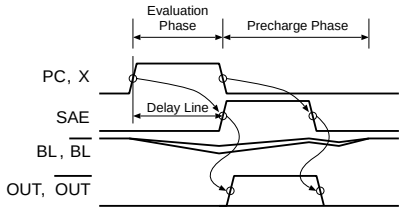

Figure 4. Timing diagram of the control signals.

The logic cells realize any 2-input Boolean function of two adjacent signals by connecting some local wires, and does not affect the circuit performance and area. Logical AND and OR of the outputs of the logic cells can be obtained from the outputs of an AND-plane and an OR-plane, respectively. Thus, the proposed PLA can realize the LC-AND-LC-OR structure, i.e., 4-level implementation in logic, but 2-level implementation in structure.

In the next section, the circuit design of the proposed PLA is described in detail.

3. Circuit Design

3.1. Basic Circuit

Figure 2 shows the basic circuit of the proposed PLA. The circuit consists of a stack of logic cells, a reference cell, a virtual ground (VG) controller, a precharge and equalization cell, and a sense amplifier. Logical OR and NOR of the outputs of the logic cells can be obtained from the output signals, OUT and $\overline{\text{OUT}}$, respectively. A logical AND is also obtained by performing a logical NOR of complement signals. Thus, an AND-plane and an OR-plane for a PLA can be realized by arranging the basic circuits. The output signals are activated by sensing the differential voltage of the dual-rail bit-line, BL and $\overline{\text{BL}}$. The purpose of dummy devices, of which the gate terminals are connected to ground, is to balance the load capacitances of BL and $\overline{\text{BL}}$. VG [7] is provided to reduce the voltage swing of the bit-lines.

The logic cells used for the basic circuit are shown in Figure 3. In addition to 1-input logic cells ((1)–(2)), the logic cells contain ten 2-input logic cells ((3)–(12)) which realize any 2-input Boolean function. The logic cells (7)–(12) are composed of pass-transistors where VG is not used. These cells do not affect the circuit performance and area. Since the logic cells (3)–(6) are composed of the logic cells (1)–(2), the logic cells (1)–(2) are used for the design.

Figure 4 shows a timing diagram of the control signals. The basic circuit operates in two phases: the precharge phase and the evaluation phase. In the precharge phase, the PC signal and all the primary inputs, X_1 to X_n, are low. Thus, the bit-lines are precharged high and equalized. At the same time, the VG node is discharged low. When the PC signal becomes high and the primary inputs are activated, the circuit enters the evaluation phase.

In the evaluation phase, $\overline{\text{BL}}$ is pulled down by charge sharing with the VG node through the reference cell every cycle. When at least one of the logic cells pulls BL down, the voltage potential of BL becomes lower than that of $\overline{\text{BL}}$ as shown in Figure 4. Otherwise, BL stays high. This is because the device size of the logic cells is designed as W, while the device size of the reference cell is $0.5W$ as shown in Figure 2. This half-size device is provided to avoid the meta-stable condition, which may be caused when there is no pull-down path on BL. The SAE signal is activated when the developed voltage difference between the bit-lines becomes larger than the designed sense volt-

Table 1. Results of logic synthesis ("time" is CPU time on Pentium III (600 MHz) for synthesis).

circuit	AND-OR		LC-AND-OR		AND-LC-OR		LC-AND-LC-OR	
	# product terms	time (sec)	# product terms	time (sec)	# product terms	time (sec)	# product terms	time (sec)
Z5xp1	65	0.1	53	0.1	62	0.6	52	2.0
add6	355	0.5	37	0.1	325	93.2	37	1.5
addm4	200	0.4	109	0.3	193	4.9	99	13.4
adr4	75	0.1	17	0.0	69	0.7	17	0.1
dist	123	0.1	75	0.1	120	2.3	70	4.8
f51m	77	0.1	51	0.1	69	0.4	48	2.0
l8err	52	0.1	39	0.0	49	0.6	38	1.0
m181	42	0.1	30	0.1	40	0.2	28	14.6
mlp4	128	0.2	97	0.1	124	1.3	92	25.6
rd73	127	0.0	37	0.0	113	5.0	34	1.4
root	57	0.1	42	0.0	52	0.9	40	1.4
sqr6	49	0.0	42	0.0	49	0.1	40	0.3
total	1350	1.8	629	0.9	1265	110.2	595	68.1

Table 2. Comparison between different implementation styles of the example circuit.

Circuit	# product terms	Area (μm^2)	Delay (ns)	Power consumption (mW) @ 80 MHz	ADP product*
Conventional single-rail PLA [5]	220	490,965	4.19	99	1.00
Conventional dual-rail PLA [7]	220	939,798	1.52	73	0.512
Proposed PLA	136	601,624	1.39	43	0.177

*(Area) $\times$ (Delay) $\times$ (Power consumption)

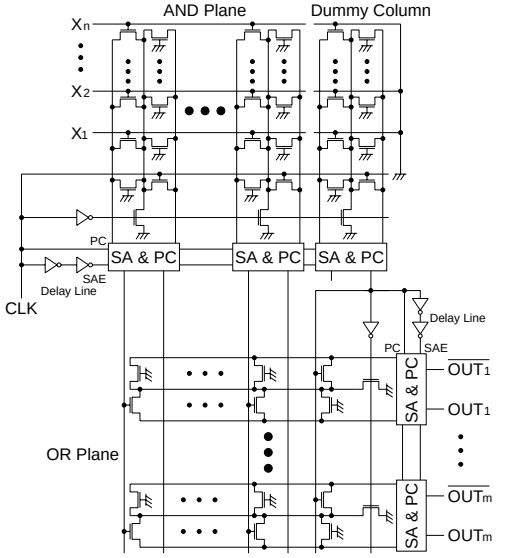

Figure 5. PLA configuration.

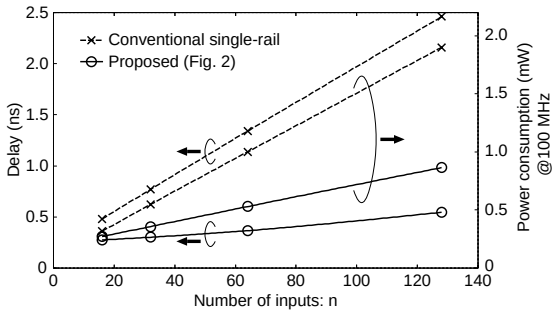

Figure 6. Basic circuit comparison for delay and power consumption (0.35-μm CMOS technology, 3.3-V V_{DD}).

age of 200 mV, which takes the worst cases of considerable noise margin and process variations into account.

3.2. PLA Configuration

The proposed PLA configuration using the basic circuits is shown in Figure 5. An array of the basic circuits is used for an AND-plane and an OR-plane. Control signals for an AND-plane are generated from the CLK signal with a delay line of a chain of sized inverters. On the other hand, control signals for an OR-plane are generated from a dummy column and a delay line of a chain of sized inverters. The dummy column is designed so that its output signal arrives last in an AND-plane. The output signal of the dummy column is activated every cycle and follows the output signals of an AND-plane across operating conditions and process variations.

4. Area and Performance Evaluation

We have already proposed a method of logic synthesis for LC-AND-LC-OR logic structures [8], [9]. By using this method, the area advantage over the conventional design has been demonstrated. Table 1 shows the results on the `math` PLA benchmark circuits [10]. In this table, LC-AND-OR, AND-LC-OR, and LC-AND-LC-OR correspond to PLAs which have the 2-input logic cells in an AND-plane, an OR-plane, and both planes, respectively. Minimizing the number of product terms (i.e., the number of basic circuits in an AND-plane) results in reducing the overall area of PLA. The results show that the LC-AND-LC-OR type PLA can realize the Boolean functions in the least number of product terms among the four types of PLAs. In particular, the results indicate that the proposed PLA is suitable for arithmetic circuits, such as

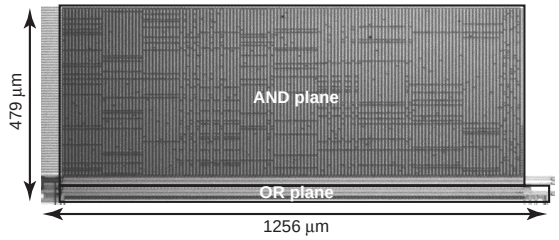

Figure 7. Chip microphotograph.

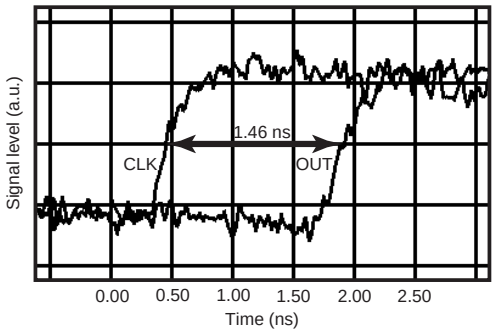

Figure 8. Measured waveforms.

add6, which are difficult to be implemented in the conventional design [6].

In our approach, a dual-rail structure is utilized. While requiring a large circuit area compared to a single-rail structure, a dual-rail structure can achieve a high-speed operation and improve the common-mode noise immunity. The area overhead can be alleviated by our method as discussed above. Figure 6 shows a simulated comparison of delay and power consumption of the proposed circuit and the conventional dynamic single-rail circuit [5]. The simulation was carried out for the basic circuit in Figure 2 and a single column circuit in AND-plane in the conventional PLA. As can be seen from this figure, the proposed circuit achieves a high-speed operation and the circuit performance can be further enhanced by reducing the number of inputs. Note that the reduction of the number of product terms leads to the reduction of the number of inputs. Moreover, by reducing the voltage swing of bit-lines, a low-power operation is also achieved in the proposed scheme. Thus, the proposed PLA is effective in terms of a lot of aspects, i.e., area, speed, and power consumption.

Table 2 shows a comparison between different implementation styles of an example circuit. The circuits were designed using a 0.35-μm CMOS technology with a supply voltage of 3.3 V. The example circuit has 64-bit inputs and a 1-bit output, and its logic function was generated randomly. The performances were obtained from post-layout simulations using HSPICE. By using the proposed scheme, the number of product terms has been reduced from 220 to 136. The proposed circuit achieves a high-speed and low-power operation, and significant reductions of area-delay-power (ADP) product by 82% and 65% compared to the conventional dynamic single-rail [5] and dual-rail PLAs [7], respectively.

5. Experimental Results

The proposed PLA in Table 2 was fabricated using a 0.35-μm, 3-metal CMOS technology with a supply voltage of 3.3 V. A chip microphotograph is shown in Figure 7. Figure 8 shows the measured waveforms for a delay measurement using an electron beam probe at room temperature. The delay from the CLK signal to the output of the PLA was 1.46 ns. The measured results show that the proposed PLA operates correctly.

6. Conclusion

In this paper, a dual-rail PLA with 2-input logic cells has been presented. By using the 2-input logic cells, some classes of logic function can be implemented in a smaller circuit area, so that a high-speed and low-power operation has been also achieved. The measured results show that the proposed PLA operates correctly. Because of a high-speed and low-power operation with a small chip area and the high predictability of performance, area, and noise, it will be a strong candidate as the preferable design methodology in the DSM era.

7. Acknowledgment

The VLSI chip in this study has been designed with CAD tools of Avant! Corp. and Cadence Design Systems Inc., and fabricated through VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Rohm Corp. and Toppan Printing Corp.

8. References

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