IEICE TRANS. ELECTRON., VOL.E87–C, NO.2 FEBRUARY 2004

PAPER

A Logic-Cell-Embedded PLA (LCPLA): An Area-Efficient Dual-Rail Array Logic Architecture

Hiroaki YAMAOKA[†a)], ***Student Member***, **Hiroaki YOSHIDA**[†], ***Nonmember***,
Makoto IKEDA[†], ***and*** **Kunihiro ASADA**[†], ***Members***

SUMMARY This paper describes an area-efficient dual-rail array logic architecture, a logic-cell-embedded PLA (LCPLA), which has 2-input logic cells in the structure. The 2-input logic cells composed of pass-transistors can realize any 2-input Boolean function and are embedded in a dual-rail PLA. The logic cells can be designed by connecting some local wires and do not require additional transistors over logic cells of the conventional dual-rail PLA. By using the logic cells, some classes of logic functions can be implemented efficiently, so that high-speed and low-power operations are also achieved. The advantages over the conventional PLAs and standard-cell-based designs were demonstrated by using benchmark circuits, and the LCPLA is shown to be effective to reduce the number of product terms. In a structure with a 64-bit input and a 1-bit output including 220 product terms, the LCPLA achieved an area reduction by 35% compared to the conventional high-speed dual-rail PLA, and the power-delay product was reduced by 74% and 46% compared to the conventional high-speed single-rail PLA and the conventional high-speed dual-rail PLA, respectively. A test chip of this configuration was fabricated using a 0.35-μm, 3-metal-layer CMOS technology, and was verified with a functional test using a logic tester and an electron-beam tester at frequencies of up to 100 MHz with a supply voltage of 3.3 V.

key words: *PLA, logic cell, dual-rail, array logic, area-efficient*

1. Introduction

In the past three decades, *programmable logic arrays* (PLAs) have been widely used for combinational and sequential logic circuits because of its simplicity, regularity, and flexibility. These features are becoming more and more important in recent complicated VLSI systems, where regular structures and simple designs are required in order to shorten design and test time. For example, control logic of the IBM 1-GHz 64-bit PowerPC processors, *Rivina* [1] and *guTS* [2], has been realized in PLAs to reduce the design complexity. The design methodology using PLAs does not require the iteration of the design process because structured arrays give predictable area, delay, and power consumption early in the design process. Thus, the design does not suffer from the so-called timing closure problem associated with synthesis, technology mapping, placement, and routing, which is often the case with recent standard-cell-based designs. In addition, the issues of signal integrity such as cross-talk noise, which are becoming increasingly serious in deep sub-micron IC designs, can be easily predicted and alleviated by taking advantage of the regularity of PLA [3]. This enables to shrink device sizes and power supply levels, as well as an increase in operating speed, with large noise margins.

In this paper, we propose an area-efficient dual-rail array logic architecture, a logic-cell-embedded PLA (LCPLA), which has 2-input logic cells in the structure. In general, though the structural regularity of PLA offers design simplicity, it requires a large chip area due to low area-efficiency. To overcome this drawback, a network structure of small PLAs which implements Boolean functions efficiently has been proposed [3]. However, this structure degrades the circuit performance due to an increase in logic levels. Besides, though each PLA is surely regular, the global regularity is sacrificed because of placement and routing. Actually, it may be even worse than that in standard-cell-based designs that have a row structure, and thus it is difficult to take advantage of the regularity of PLA. In our approach, 2-input logic cells which realize any 2-input Boolean function can be embedded in a dual-rail PLA. The logic cells can be designed by connecting some local wires and do not require additional transistors over logic cells of the conventional dual-rail PLA [4]. By using the logic cells, some classes of logic functions can be implemented efficiently, so that high-speed and low-power operations are also achieved due to the reduction of circuit elements.

This paper is organized as follows. In Sect. 2, the circuit design of LCPLA is described. Section 3 discusses the advantages of LCPLA over the conventional designs. Measurement results of a test chip are presented in Sect. 4. Finally, conclusions are drawn in Sect. 5.

2. Circuit Design

Figure 1 shows a structure of LCPLA. The structure has a dual-rail configuration. The X_i and $\overline{X_i}$ signals are the primary input and its negation, respectively. The OUT_j and $\overline{OUT_j}$ signals are the outputs of the PLA. An LCPLA contains an AND-plane and an OR-plane, and is capable of implementing any Boolean function expressed in a sum-of-products form by connecting switching transistors, which are denoted by dots in the figure, to the input and output wires. In addition, an LCPLA utilizes 2-input logic cells (LCs) in both planes. The 2-input logic cells realize any 2-input Boolean function of two adjacent signals and are embedded in the PLA to reduce chip area. These logic cells can

Manuscript received March 25, 2003.
Manuscript revised August 13, 2003.

[†]The authors are with the Department of Electronics Engineering, and VLSI Design and Education Center (VDEC), The University of Tokyo, Tokyo, 113-8656 Japan.
a) E-mail: yamaoka@silicon.u-tokyo.ac.jp

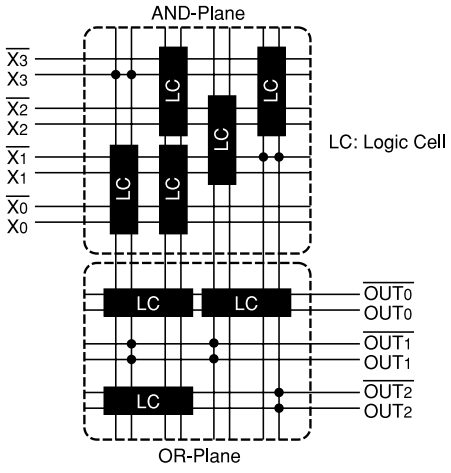

Fig. 1 LCPLA structure.

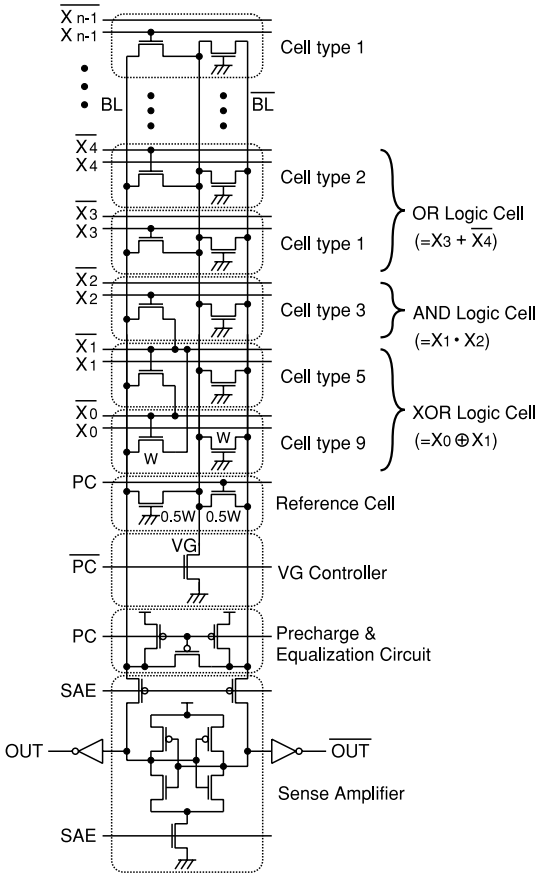

Fig. 2 Basic circuit of LCPLA.

be easily designed from the original logic cell by connecting some local wires. Logical AND and OR of the outputs of the logic cells can be obtained from the outputs of AND-plane and OR-plane, respectively. Thus, an LCPLA can realize an LC-AND-LC-OR structure, i.e., 4-level logic implementation.

Figure 2 shows a basic circuit of LCPLA, which is used as a column circuit in an AND-plane and an OR-plane. The

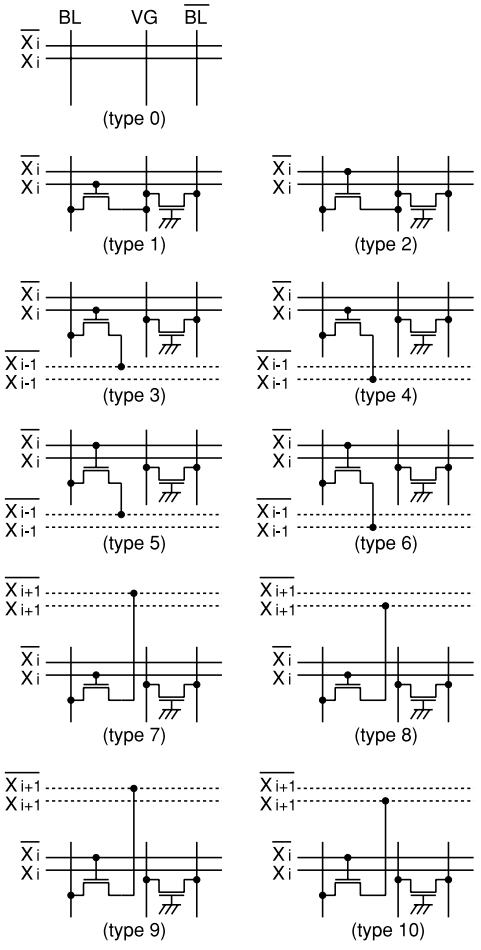

Fig. 3 Basic logic cells.

circuit has a dual-rail configuration and consists of a stack of the basic logic cells shown in Fig. 3, a reference cell, a virtual ground (VG) controller, a precharge and equalization circuit, and a sense amplifier. Logical OR and NOR of the outputs of the basic logic cells can be obtained from the output signals, OUT and $\overline{OUT}$, respectively. A logical AND is also obtained by performing a logical NOR of complement signals. Thus, an AND-plane and an OR-plane for a PLA can be realized by arranging the basic circuits. By using a sense amplifier, the output signals are activated by sensing the differential voltage between the bit-lines, BL and $\overline{\text{BL}}$. VG is provided to reduce the voltage swings of the bit-lines.

There are 11 basic logic cells, which can be embedded in a basic circuit, as shown in Fig. 3. Each cell has a pair of NMOS devices, except for type 0. One is used to pull down the bit-line (BL) depending on the input signals (X_0–X_{n-1}). The other is to balance the load capacitances and leakage current of BL and $\overline{\text{BL}}$. This symmetrical structure results in a robust operation of the circuit, especially with respect to common-mode noise. The basic cells of type 3–10 are composed of pass-transistors and are realized by connecting some local wires. By using the basic logic cells, the logic function of a basic circuit is expressed as

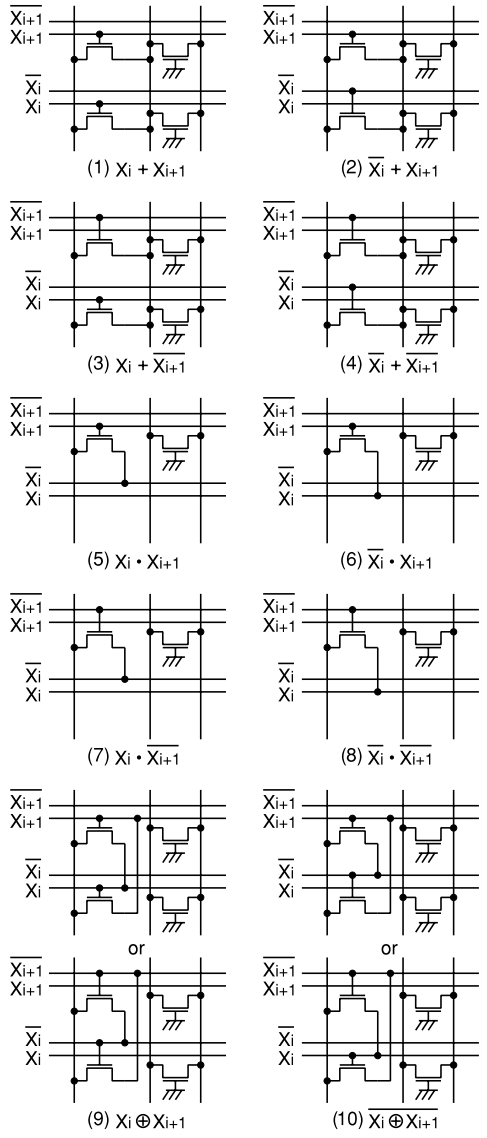

Fig. 4 2-input logic cells (LCs) using the basic logic cells.

$$OUT = \sum_{i=0}^{n-1} Y_i \tag{1}$$

$$Y_i = \begin{cases} 0 & \cdots \text{ type 0} \\ X_i & \cdots \text{ type 1} \\ \overline{X_i} & \cdots \text{ type 2} \\ X_i \cdot X_{i-1} & \cdots \text{ type 3 } (i \neq 0) \\ X_i \cdot \overline{X_{i-1}} & \cdots \text{ type 4 } (i \neq 0) \\ \overline{X_i} \cdot X_{i-1} & \cdots \text{ type 5 } (i \neq 0) \\ \overline{X_i} \cdot \overline{X_{i-1}} & \cdots \text{ type 6 } (i \neq 0) \\ X_i \cdot X_{i+1} & \cdots \text{ type 7 } (i \neq n-1) \\ X_i \cdot \overline{X_{i+1}} & \cdots \text{ type 8 } (i \neq n-1) \\ \overline{X_i} \cdot X_{i+1} & \cdots \text{ type 9 } (i \neq n-1) \\ \overline{X_i} \cdot \overline{X_{i+1}} & \cdots \text{ type 10 } (i \neq n-1) \end{cases} \tag{2}$$

where Y_i is a logic function realized by the basic logic cell and corresponds to the type of the basic logic cell.

2-input logic cells using the basic logic cells are shown in Fig. 4. By combining the basic logic cells, arbitrary 2-input logic functions of two adjacent signals can be realized. The 2-input logic cells of (1)–(4), which realize logical OR, are formed by the basic logic cells of type 1–2. On the other hand, the 2-input logic cells of (5)–(8), which realize logical AND, are formed by the basic logic cells of type 3–6. The 2-input logic cells of (9)–(10), which realize logical XOR and XNOR, have two configurations, respectively, and are formed by the basic logic cells of type 3–10. These cells do not degrade the circuit area because pass-transistors used in the structure give no additional area. Thus, the resulting circuits cannot be worse in terms of area over the conventional dual-rail PLA [4].

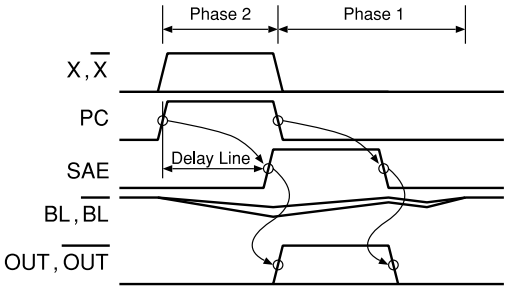

Fig. 5 Timing diagram of control signals, input and output signals, and bit-line potentials in a basic circuit.

Figure 5 shows a timing diagram of control signals, input and output signals, and bit-line potentials in a basic circuit. The circuit operates in two phases: phase 1 and phase 2. In phase 1, the PC signal and all the primary inputs, X_0–X_{n-1} and $\overline{X_0}$–$\overline{X_{n-1}}$, are low. Thus, the bit-lines are precharged high and equalized. At the same time, the VG node is discharged low. When the PC signal becomes high and the primary inputs are activated, the circuit enters phase 2.

In phase 2, $\overline{BL}$ is pulled down by charge sharing with VG through the reference cell. When at least one of the basic logic cells pulls BL down, the voltage potential of BL becomes lower than that of $\overline{BL}$. Otherwise, BL stays high. This is because the device size of the basic logic cells is W, while that of the reference cell is $0.5W$ as shown in Fig. 2, where W is the channel width of a transistor. This half-size device is provided to avoid the meta-stable condition, which may be caused when there is no pull-down path on BL. The SAE signal is activated when the developed voltage difference between the bit-lines becomes larger than the designed sense voltage of 200 mV, which takes the worst case of considerable noise margin and process variations into account. By activating the sense amplifier, one of the output signals, i.e., OUT or $\overline{OUT}$ becomes high depending on the developed voltage difference. After the activation of the sense amplifier, the PC signal becomes low and the circuit starts to precharge the bit-lines.

Also, in phase 2, short-circuit current between input wires may be caused depending on the combinations of the basic logic cells. For example, when the state of ($\overline{X_0}$, $\overline{X_1}$, X_2) = (low, high, high) arises in the circuit of Fig. 2, $\overline{X_0}$ pulls BL

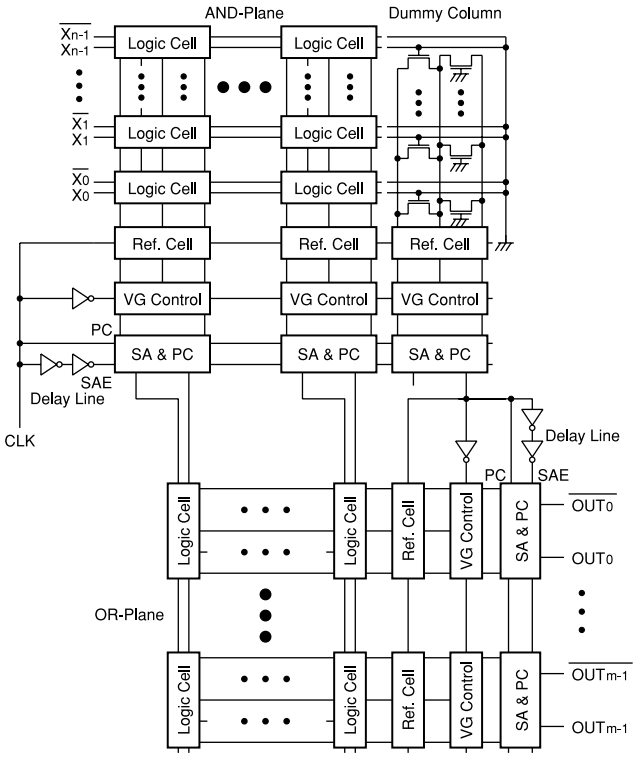

Fig. 6 Overall configuration of LCPLA.

down via the pass-transistor controlled by $\overline{X_1}$. At the same time, $\overline{X_1}$ tries to drive BL into high via the pass-transistor controlled by X_2. Thus, this makes a current path from $\overline{X_1}$ to $\overline{X_0}$. However, short-circuit current between the input wires is caused only when the voltage potential of BL becomes lower than $V_{DD} - V_t$ because an NMOS transistor is used as a pull-up device in this case, where V_{DD} is the power supply voltage and V_t is the threshold voltage of the transistor. This also means that the basic logic cells never drive BL into V_{DD}. Moreover, the threshold voltage (V_t) of the pull-up device is not constant with respect to the voltage difference between the substrate and the source of the transistor, and is enhanced because the source of the pull-up device is precharged high. This is known as the *body effect* [5] and helps to reduce the short-circuit current. Also, when avoiding the short-circuit current is required, which is often the case with systems where power consumption is the primary concern, it is realized by introducing a restriction in how to combine the basic logic cells, i.e., by avoiding two or more 2-input logic cells using pass-transistors in a basic circuit. We evaluated and confirmed operations of LCPLAs, which take all possible cases of the combinations of the basic logic cells into account, in various logic functions in the following sections.

The overall configuration of LCPLA is shown in Fig. 6. An array of basic circuits is used as an AND-plane and an OR-plane. Control signals of the AND-plane are generated from the CLK signal with a delay line of a chain of sized inverters. On the other hand, control signals of the OR-plane are generated from a dummy column and a delay line of a chain of sized inverters. The dummy column is designed so that its output signal arrives last in the AND-plane. For this purpose, it has the largest number of basic logic cells in the AND-plane, and gate terminals of the basic logic cells are connected to ground. Its output signal, i.e., the PC signal of the OR-plane is activated every cycle and follows operating conditions, such as temperature and supply voltage variations, as well as process variations in sync with the AND-plane.

3. Area and Performance Evaluation

In order to implement a given logic function into the proposed PLA, we proposed a method of logic synthesis for LC-AND-LC-OR logic structures [6]. By implementing the method as a part of ESPRESSO-MV [7], the area advantage over the conventional structure was demonstrated.

Table 1 shows the results of logic synthesis on the math PLA benchmark circuits [8]. In this table, LC-AND-OR, AND-LC-OR, and LC-AND-LC-OR correspond to PLAs which have 2-input logic cells in AND-plane, OR-plane, and both planes, respectively. In the design of a PLA, minimizing the number of product terms (i.e., the number of basic circuits in AND-plane) results in reducing the overall area. Also, an LCPLA can be implemented in the same area as the conventional dual-rail PLA [4] even if the number of product terms can not be reduced by using 2-input logic cells. The results show that the LC-AND-LC-OR structure can realize the Boolean functions in the least number of product terms among the four types of PLAs. In particular, the results indicate that the LCPLA is suitable for arithmetic circuits, such as add6, which are difficult to be implemented in the conventional PLA [9]. By using LC-AND-LC-OR structures, the number of product terms was reduced by 56% on average compared to that in AND-OR structures.

Table 2 shows a comparison of standard-cell-based design and LCPLA on the math PLA benchmark circuits [8]. Each circuit was designed using a 0.35-μm, 3-metal-layer CMOS technology with a supply voltage of 3.3 V. Logic synthesis of standard-cell-based design was performed using Synopsys Design Compiler with delay priority and 395 standard cells. The standard cells are based on the Rohm 0.35-μm CMOS technology and are provided by VLSI Design and Education Center (VDEC) [10]. The synthesized circuits were placed and routed using Synopsys Apollo. The delay and power characteristics of standard-cell-based design were obtained by the timing and power analysis of Synopsys Design Compiler with wire load information, which is given by placement and routing, while the area characteristics were obtained by physical layouts after placement and routing. On the other hand, the delay and power characteristics of LCPLA were obtained by post-layout simulations using HSPICE, where LC-AND-LC-OR structures were used. Also, the area characteristics represent physical layouts of LC-AND-LC-OR structures. The results show that the LCPLA requires on average 3.29 times the area of the standard-cell-based design. This is mainly because

Table 1 Results of logic synthesis ("Time" is CPU time on Pentium III (600 MHz) processor for synthesis).

Circuit	AND-OR		LC-AND-OR		AND-LC-OR		LC-AND-LC-OR	
	# product terms	Time (sec)	# product terms	Time (sec)	# product terms	Time (sec)	# product terms	Time (sec)
Z5xp1	65	0.1	53	0.1	62	0.6	52	2.0
add6	355	0.5	37	0.1	325	93.2	37	1.5
addm4	200	0.4	109	0.3	193	4.9	99	13.4
adr4	75	0.1	17	0.0	69	0.7	17	0.1
dist	123	0.1	75	0.1	120	2.3	70	4.8
f51m	77	0.1	51	0.1	69	0.4	48	2.0
l8err	52	0.1	39	0.0	49	0.6	38	1.0
m181	42	0.1	30	0.1	40	0.2	28	14.6
mlp4	128	0.2	97	0.1	124	1.3	92	25.6
rd73	127	0.0	37	0.0	113	5.0	34	1.4
root	57	0.1	42	0.0	52	0.9	40	1.4
sqr6	49	0.0	42	0.0	49	0.1	40	0.3
Total	1350	1.8	629	0.9	1265	110.2	595	68.1
Ratio	1.00	1.00	0.466	0.500	0.937	61.2	0.441	37.8

Table 2 Comparison of standard-cell-based design and LCPLA.

Circuit	Area (μm^2)		Delay (ns)		Power (mW) @ 200 MHz		PD product (pJ)	
	Std-cell	This work	Std-cell	This work	Std-cell	This work	Std-cell	This work
Z5xp1	14,042	83,785	1.22	0.69	7.8	23.0	9.52	15.87
add6	17,110	68,507	1.28	0.68	10.2	16.9	13.06	11.49
addm4	56,608	143,503	1.53	0.74	30.4	45.2	46.51	33.45
adr4	5,561	32,727	0.94	0.65	3.3	8.0	3.10	5.20
dist	47,306	90,381	1.64	0.71	24.6	30.5	40.34	21.66
f51m	14,042	75,429	1.12	0.69	8.2	21.6	9.18	14.90
l8err	15,812	63,081	1.36	0.67	8.6	17.2	11.70	11.52
m181	10,700	65,832	0.83	0.67	5.9	14.2	4.90	9.51
mlp4	47,306	129,760	1.32	0.73	24.0	39.6	31.68	28.91
rd73	18,088	44,463	1.15	0.67	10.7	15.2	12.31	10.18
root	19,418	57,747	1.28	0.68	10.9	17.7	13.95	12.04
sqr6	15,340	71,124	1.07	0.67	8.6	19.3	9.20	12.93
Total	281,333	926,339	14.74	8.25	153.2	268.4	205.45	187.66
Ratio	1.00	3.29	1.00	0.560	1.00	1.75	1.00	0.913

of dual-rail structures and the difference of area-efficiency between regular and random structures. The delay of the LCPLA is on average 0.560 times that of the standard-cell-based design. In addition to the high-speed capability of sense amplifiers in the proposed structure, the LCPLA implements logic functions in 2-level logic forms with 2-input logic cells and thus results in having superior delay characteristics. In the standard-cell-based design, the increase in delay is incurred in traversing the different logic levels of the design. Moreover, the maximum delay of the standard-cell-based design is 1.64 ns (dist), while the minimum delay is 0.83 ns (m181). Thus, the maximum difference of delay between each circuit is 0.81 ns. On the other hand, the maximum delay of the LCPLA is 0.74 ns (addm4), while the minimum delay is 0.65 ns (adr4). Thus, the difference of delay between each circuit is limited only within 0.09 ns. Also, the worst case delay of LCPLA can be easily obtained from the delay of the basic circuit having a maximally loaded bit-line. This feature of LCPLA makes the circuit delay predictable early in the design process, and thus it is possible to eliminate the ambiguity of the design and to alleviate the timing closure problem. The power consumption of the LCPLA is

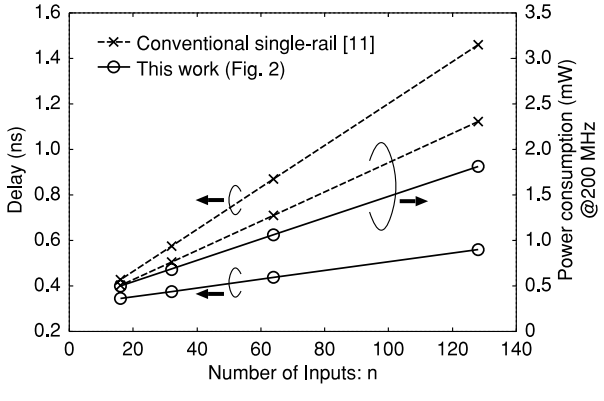

Fig. 7 Basic circuit comparison in terms of delay and power consumption (0.35-μm CMOS technology, 3.3-V power supply).

on average 1.75 times that of the standard-cell-based design. This is mainly because input signal wires and bit-lines are charged and discharged every cycle. The power-delay (PD) product of the LCPLA is on average 0.913 times that of the standard-cell-based design.

In our approach, a dual-rail structure is utilized. A

Table 3 Comparison of the conventional PLAs and LCPLA.

Circuit (64-bit input, 1-bit output)	Configuration	Area (μm^2)	Delay (ns)	Power (mW) @ 80 MHz	PD product (normalized)
Domino circuit [5]	single-rail	489,440	3.56	95	1.00
Blair et al. [12]	single-rail	489,582	3.08	405	3.69
Dhong et al. [13]	single-rail	492,048	2.80	176	1.46
Wang et al. [11]	single-rail	498,078	2.56	92	0.696
Yamaoka et al. [4]	dual-rail	939,798	1.52	73	0.328
This work (LC-AND-LC-OR)	dual-rail	601,624	1.39	43	0.177

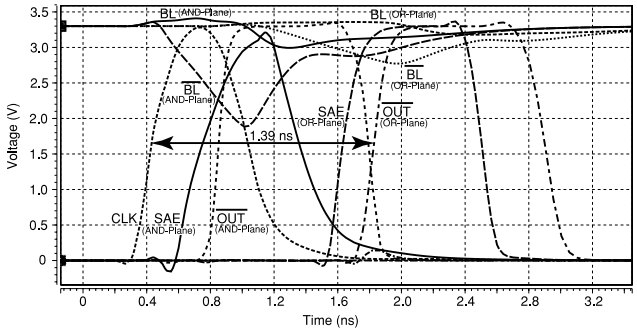

Fig. 8 Simulated waveforms of the LCPLA.

dual-rail structure can achieve a high-speed operation and improve the common-mode noise immunity, while requiring a large circuit area compared to a single-rail structure. The area overhead can be reduced by our method as discussed above. Figure 7 shows a comparison of delay and power consumption of the proposed circuit and the conventional high-speed and low-power single-rail circuit [11]. Simulations were carried out for the basic circuit in Fig. 2 and a single column circuit in an AND-plane in the conventional single-rail PLA [11]. The circuits were designed using a 0.35-μm, 3-metal-layer CMOS technology with a supply voltage of 3.3 V, and the performances were obtained from post-layout simulations using HSPICE. As can be seen from this figure, both the circuit delay and power consumption of each circuit increase in proportion to the number of inputs. The results show that the proposed circuit can achieve a high-speed operation, especially in the circuit with a large number of inputs, over the conventional single-rail circuit, and the circuit performance can be further enhanced by reducing the number of inputs. Note that the reduction of the number of product terms leads to the reduction of the number of inputs in an OR-plane. Moreover, by reducing voltage swings of bit-lines, a low-power operation is also achieved in the proposed scheme. The proposed circuit with a 64-bit input can reduce delay and power consumption by 49% and 16%, respectively, compared to the conventional high-speed and low-power single-rail circuit [11].

Table 3 shows a comparison of the conventional PLAs and LCPLA. In order to compare the conventional PLAs with LCPLA, we designed an example circuit using a 0.35-μm, 3-metal-layer CMOS technology with a supply voltage of 3.3 V. The example circuit has a 64-bit input and a 1-bit output, and its logic function was generated randomly. The generated logic function was optimized using ESPRESSO [8] before implementation. The number of product terms and the number of logic cells in the optimized logic function are 220 and 3,368, respectively. This circuit scale is relatively large over the PLA benchmark circuits [8], and the circuit becomes a good criterion as a large PLA, which suits the recent microprocessors [1], [2]. Also, since area, delay, and power consumption of a PLA mainly depend on the numbers of product terms and logic cells if the numbers of inputs and outputs are fixed, we can see how much the reductions of the numbers of product terms and logic cells affect on these circuit characteristics by using the example circuit. The performances were obtained from post-layout simulations using HSPICE. Simulated waveforms of the LCPLA are shown in Fig. 8. By using an LC-AND-LC-OR structure, the number of product terms was reduced from 220 to 136 (38% reduction) and the number of basic logic cells was reduced from 3,368 to 2,042 (39% reduction). As a result, the proposed circuit achieved an area reduction by 35% compared to the conventional high-speed dual-rail PLA [4]. Also, the circuit delay and power consumption of the LCPLA are the smallest among all of the PLAs in Table 3, and the power-delay (PD) product was reduced by 74% and 46% compared to the conventional high-speed single-rail PLA [11] and the conventional dual-rail PLA [4], respectively.

4. Measurement Results

The LCPLA in Table 3 was fabricated using a 0.35-μm, 3-metal-layer CMOS technology. A chip microphotograph is shown in Fig. 9, which includes 136 and 1 basic circuits in the AND-plane and the OR-plane, respectively. The physical dimension is $479 \times 1{,}256\,\mu$m^2. The operations of the LCPLA were successfully verified with a functional test using a logic tester at frequencies of up to 100 MHz, which is the limitation of the test equipment, at 25°C with a supply voltage of 3.3 V.

In order to measure the propagation delay of the test chip, a delay measurement using an electron-beam tester was also performed at the same conditions as the functional test. Figure 10 shows measured waveforms along the critical path. The timebase resolution of the test equipment is 10 ps. The measured delay from the CLK signal to the output signal of the PLA was 1.46 ns, while the power consumption is 241 mW at a simulated frequency of 500 MHz. The features of the test chip are summarized in Table 4.

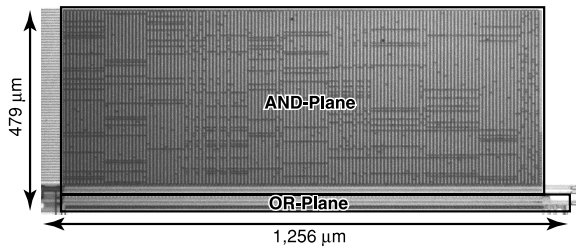

Fig. 9 Chip microphotograph of the LCPLA.

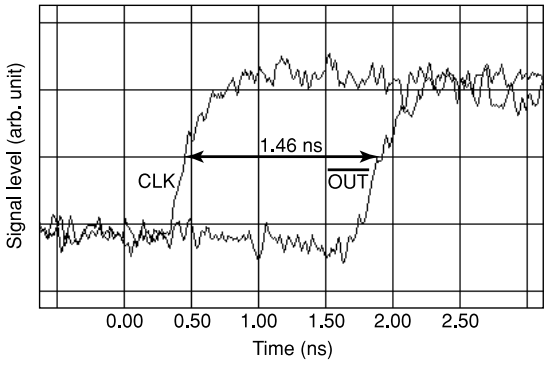

Fig. 10 Measured waveforms by an electron-beam tester.

Table 4 Features of the test chip.

Process technology	0.35-μm CMOS, 3-metal
Supply voltage	3.3 V
Transistor count	7.1 k
# product terms	136
# basic logic cells (AND-plane)	1,906
# basic logic cells (OR-plane)	136
Physical dimension	$479 \times 1{,}256\,\mu m^2$
Simulated cycle time	1.98 ns (500 MHz)
Simulated power consumption	241 mW (@ 500 MHz)
Measured delay time	1.46 ns

5. Conclusions

In this paper, an area-efficient dual-rail array logic architecture, a logic-cell-embedded PLA (LCPLA), was presented. By embedding 2-input logic cells in the structure, some classes of logic functions can be implemented efficiently, so that high-speed and low-power operations were also achieved. The logic cells can be designed by connecting some local wires and do not require additional transistors over logic cells of the conventional dual-rail PLA. The advantages over the conventional PLAs and standard-cell-based designs were demonstrated by using benchmark circuits, and the LCPLA is shown to be effective to reduce the number of product terms. In a structure with a 64-bit input and a 1-bit output including 220 product terms, the LCPLA achieved an area reduction by 35% compared to the conventional high-speed dual-rail PLA, and the power-delay product was reduced by 74% and 46% compared to the conventional high-speed single-rail PLA and the conventional high-speed dual-rail PLA, respectively. A test chip of this configuration was fabricated using a 0.35-μm, 3-metal-layer CMOS technology, and was verified with a functional test using a logic tester and an electron-beam tester at frequencies of up to 100 MHz with a supply voltage of 3.3 V. Because of the high-speed capability with the high area-efficiency and the high predictability of performance, area, and signal integrity, the proposed PLA will be a preferable design methodology in the deep sub-micron era.

Acknowledgment

The VLSI chip in this study has been designed with CAD tools of Synopsys, Inc. and Cadence Design Systems, Inc., and fabricated through the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Rohm Corp. and Toppan Printing Corp.

References

[1] S. Posluszny, N. Aoki, D. Boerstler, P. Coulman, S. Dhong, B. Flachs, P. Hofstee, N. Kojima, O. Kwon, K. Lee, D. Meltzer, K. Nowka, J. Park, J. Peter, J. Silberman, O. Takahashi, and P. Villarrubial, ""Timing closure by design," a high frequency microprocessor design methodology," Proc. Design Automation Conf., pp.712–717, 2000.

[2] S. Posluszny, N. Aoki, D. Boerstler, J. Burns, S. Dhong, U. Ghoshal, P. Hofstee, D. LaPotin, K. Lee, D. Meltzer, H. Ngo, K. Nowka, J. Silberman, O. Takahashi, and I. Vo, "Design methodology for a 1.0 GHz microprocessor," Proc. IEEE Int. Conf. Computer Design, pp.17–23, 1998.

[3] S. Khatri, R. Brayton, and A. Sangiovanni-Vincentelli, "Cross-talk immune VLSI design using a network of PLAs embedded in a regular layout fabric," Proc. Int. Conf. Computer-Aided Design, pp.412–418, 2000.

[4] H. Yamaoka, M. Ikeda, and K. Asada, "A high-speed PLA using array logic circuits with latch sense amplifiers and a charge sharing scheme," Proc. IEEE Asia and South Pacific Design Automation Conf., pp.3–4, 2001.

[5] N. Weste and K. Eshraghian, Principles of CMOS VLSI Design: A Systems Perspective, 2nd ed., Addison Wesley, Boston, MA, 1993.

[6] H. Yoshida, H. Yamaoka, M. Ikeda, and K. Asada, "Logic synthesis for PLA with 2-input logic elements," Proc. IEEE Int. Symp. Circuits and Systems, vol.3, pp.373–376, 2002.

[7] R. Rudell and A. Sangiovanni-Vincentelli, "Multiple-valued minimization for PLA optimization," IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst., vol.CAD-6, no.5, pp.727–750, Sept. 1987.

[8] R. Brayton, G. Hachtel, C. McMullen, and A. Sangiovanni-Vincentelli, Logic Minimization Algorithms for VLSI Synthesis, Kluwer Academic Publishers, Boston, MA, 1984.

[9] M. Schmookler, "Design of large ALUs using multiple PLA macros," IBM J. Res. & Devel., vol.24, pp.2–14, Jan. 1980.

[10] VLSI Design and Education Center, http://www.vdec.u-tokyo.ac.jp/English/index.html.

[11] C.C. Wang, C.F. Wu, R.T. Hwang, and C.H. Kao, "A low-power and high-speed dynamic PLA circuit configuration for single-clock CMOS," IEEE Trans. Circuits Syst. I, Fundam. Theory Appl., vol.46, pp.857–861, July 1999.

[12] G.M. Blair, "PLA design for single-clock CMOS," IEEE J. Solid-State Circuits, vol.27, pp.1211–1213, Aug. 1992.

[13] Y.B. Dhong and C.P. Tsang, "High speed CMOS POS PLA using predischarged OR array and charge sharing AND array," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol.39, pp.557–564, Aug. 1992.

Hiroaki Yamaoka was born in Tokyo, Japan, on October 15, 1976. He received the B.S. degree in electronics engineering from the University of Electro-Communications, Tokyo, Japan, in 1999 and the M.S. degree in electronics engineering from the University of Tokyo, Tokyo, Japan, in 2001. He is currently pursuing the Ph.D. degree in electronics engineering at the University of Tokyo. His current research interests include the design of high-performance CMOS digital circuits and logic synthesis. He is a student member of the Institute of Electrical and Electronics Engineers (IEEE).

Hiroaki Yoshida received the B.S. and M.S. degrees in electronics engineering from the University of Tokyo, Tokyo, Japan, in 2000 and 2002, respectively. Currently, he is a Software Engineer at Zenasis Technologies, Inc., Campbell, CA, where he is working on the development of a leading-edge logic/physical/transistor-level timing optimization tool. His research interests include logic- and transistor-level optimization of high-performance circuits.

Makoto Ikeda received the B.S., M.S., and Ph.D. degrees in electronics engineering from the University of Tokyo, Tokyo, Japan, in 1991, 1993, and 1996, respectively. He joined the Electronics Engineering Department, the University of Tokyo, as a faculty member in 1996 and is currently an Associate Professor at the VLSI Design and Education Center (VDEC), the University of Tokyo. His research interests include the reliability of VLSI design. He is a member of the Institute of Electrical and Electronics Engineers (IEEE) and the Information Processing Society of Japan (IPSJ).

Kunihiro Asada was born in Fukui, Japan, on June 16, 1952. He received the B.S., M.S., and Ph.D. degrees in electronics engineering from the University of Tokyo, Tokyo, Japan, in 1975, 1977, and 1980, respectively. In 1980, he joined the Faculty of Engineering, the University of Tokyo, and became a Lecturer, an Associate Professor, and a Professor in 1981, 1985, and 1995, respectively. From 1985 to 1986, he was with Edinburgh University, Edinburgh, U.K., as a Visiting Scholar supported by the British Council. From 1990 to 1992, he served as the first Editor of English version of IEICE Transactions on Electronics. In 1996, he established the VLSI Design and Education Center (VDEC) with his colleagues at the University of Tokyo. It is a center supported by the government to promote education and research of VLSI design in all the universities and colleges in Japan. He is currently in charge of the head of VDEC. His research interests are in design and evaluation of integrated systems and component devices. He has published more than 390 technical papers in journals and conference proceedings. He has received the best paper awards from the Institute of Electrical and Electronics Engineers (IEEE), the Institute of Electrical Engineers of Japan (IEEJ), and IEICE. He is a member of IEEE and IEEJ.