Curriculum Vitae

Thanyapat Sakunkonchak

Title

Postdoctoral Researcher

Office

VLSI Design and Education Center (VDEC)
University of Tokyo
2–11–16 Yayoi, Bunkyo-ku, Tokyo 113–0032 JAPAN
Phone & Fax: +81–3–5841–6764
Email: thong@cad.t.u-tokyo.ac.jp, thanyapat@gmail.com
Homepage: http://www.cad.t.u-tokyo.ac.jp/~thong/

Research Interests

Formal Verification. Hardware/Software Verification. Synchronization in Concurrent Systems. Program Analysis. Equivalence Checking.

Objective

Seeking a challenging position in research and development of formal verification tools especially ones that related to formal hardware/software verifiers and equivalence checkers.

Education

Oct. 2001 – Sep. 2004	Ph.D. in Electronics Engineering University of Tokyo, Japan
Jun. 1998 – Aug. 2001	Master in Electrical Engineering Sirindhorn International Institute of Technology (SIIT)
Jun. 1993 – Mar. 1997	Bachelor in Electrical Engineering Sirindhorn International Institute of Technology (SIIT)

Ph.D. Thesis

Title: Formal Verification of Synchronization in System-Level Design

Advisor: Professor Masahiro Fujita

Awards and Fellowships

Oct. 2006 – Sep. 2007	Research Fellowship Semiconductor Technology Academic Research Center (STARC)
Oct. 2004 – Sep. 2006	Research Fellowship Japan Society for the Promotion of Science (JSPS)
Oct. 2001 – Sep. 2004	Scholarship Japanese Government (Monbukagakusho)

Work Experiences

Oct. 2006 – Sep. 2007	Postdoctoral Researcher University of Tokyo, Japan with supported grant from STARC
Oct. 2004 – Sep. 2006	Postdoctoral Researcher University of Tokyo, Japan with supported grant from JSPS
Aug. 2002 – Nov. 2002	Internship Fujitsu Laboratory of America (FLA), CA
Apr. 1997 – Aug. 2001	Teaching and Research Assistant Sirindhorn International Institute of Technology (SIIT)
Apr. 1996 – May. 1996	Internship Read/Rite Electronics, Ayutthaya, Thailand
Mar. 1996 – Apr. 1996	Internship Sanyo Electronics, Gunma, Japan

Brief Summary

I have been researching and implementing a synchronization verification tool based on SpecC language called S-VeT. This tool applies the predicate abstraction method to produce a Boolean program and translates this Boolean program to SMV description to do model checking with NuSMV. If it turns out that this abstract model contains an error, an abstract counterexample is given. This abstract counterexample is validated whether it is feasible or not by concretizing it with the original program and performing path simulation. If this path is feasible, the real counterexample is given. Otherwise, this abstract counterexample is spurious. Once the predicate that caused infeasibility in this abstract counterexample is found, it will be used for the refinement of abstraction in the next refinement step. This is known as Counterexample-Guided Abstraction Refinement (CEGAR).

To validate synchronization, the timing constraints of all statements are used (please refer to reference [2] in conference publication). Then all these timing constraints are validated by translating into Linear Programming problem and apply Linear Programming Solver.

S-VeT is implemented in C++. Given the original program in SpecC, S-VeT can automatically find assertion errors by performing abstraction, model checking, path concretization, path simulation, predicate discovery, refinement of abstraction, and timing constraints validation.

According to the publication lists, there is no active publication record in year 2006. This is due to the reason that I was concentrating on the implementation of S-VeT.

Software

A tool for synchronization verification (S-VeT)
`http://www.cad.t.u-tokyo.ac.jp/~thong/S-VeT/`

Computer Skills

Programming Languages

C, C++, Ocaml, Java

Verification Tools

NuSMV, CVC Lite, BLAST, MAGIC, CUDD, zChaff, SLEC

Operating Systems

UNIX, Windows XP, Mac OSX

Publications

Book Chapter

1. Thanyapat Sakunkonchak and Masahiro Fujita, "Verification of Synchronization in SpecC Description with the Use of Difference Decision Diagrams," In *System Specification and Design Languages: Best of FDL'02 Ed. By Eugenio Villar and Jean P. Mermet*, Kluwer Academic Publisher, April 2003, ISBN 1-4020-7414-X.

Journal Publications

1. Thanyapat Sakunkonchak, Satoshi Komatsu and Masahiro Fujita, "Synchronization Verification in System-Level Design with ILP Solvers," In *IEICE Trans. on Special Section on VLSI Design and CAD Algorithms*, Vol.E89–A, No.12, pp.3387–3396, December 2006.
2. Thanyapat Sakunkonchak, Satoshi Komatsu and Masahiro Fujita, "Verification of Synchronization in SpecC Descriptions with the Use of Difference Decision Diagrams," In *IEICE Trans. on Special Section on VLSI Design and CAD Algorithms*, Vol.E86–A, No.12, pp.3192–3199, December 2003.
3. Thanyapat Sakunkonchak and Sawasd Tantaratana, "A high-speed multiplier-free realization of IIR filter using ROM's and elevated signal rate," In *IEICE Trans. on Fundamentals*, Vol.E84–A, No.6, pp. 1479–1487, June 2001.

Conference Publications

1. Thanyapat Sakunkonchak, Takeshi Matsumoto, Hiroshi Saito, Satoshi Komatsu, and Masahiro Fujita, "Equivalence Checking in C-based System-Level Design by Sequentializing Concurrent Behaviors," In *The 3rd IASTED International Conference on Advances in Computer Science and Technology (ACST2007)*, pp.36–42, Phuket, Thailand, April 2-4 2007.
2. Thanyapat Sakunkonchak and Masahiro Fujita, "Synchronization Verification in System-Level Design with ILP Solvers," In *Third ACM-IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE2005)*, pp.121–130, Verona Italy, July 11-14 2005.
3. Yu Liu, Thanyapat Sakunkonchak, Satoshi Komatsu and Masahiro Fujita, "System Level Design Language Extensions for Timed/Untimed Digital-Analog Com-

bined System Design," In *Proc. of ACM Great Lakes Symposium on VLSI (GLSVLSI2005)*, pp.130–133, Chicago, USA, March 2005.

4. Masahiro Fujita, Satoshi Komatsu, Thanyapat Sakunkonchak, Yoshihisa Kojima, Ken Tanabe and Takeshi Matsumoto, "CAD Techniques for Hardware/Software Co-design Targeting Space Satellites," In *Proc. of International Symposium on Electronics for Future Generations*, pp.107–112, Tokyo Japan, March 2004.
5. Thanyapat Sakunkonchak and Masahiro Fujita, "Formal Verification of Synchronization Issue in System-Level Design with Automatic Abstraction," In *IFIP International Conference on Very Large Scale Integration (IFIP VLSI-SoC 2003)*, pp.464, Darmstadt Germany, December 2003 (Ph.D. Forum).
6. Thanyapat Sakunkonchak and Masahiro Fujita, "Formal Verification of Synchronization Issues in SpecC Description with Automatic Abstraction," In *Model Checking for Dependable Software-Intensive Systems Workshop*, In *The International Conference on Dependable Systems and Networks (DSN-2003)*, pp.w67–w71, San Francisco USA, June 2003.
7. Takeshi Matsumoto, Thanyapat Sakunkonchak, Hiroshi Saito, and Masahiro Fujita, "Verification of Behavioral Consistency in C by Using Symbolic Simulation and Program Slicer," In *Model Checking for Dependable Software-Intensive Systems Workshop*, In *The International Conference on Dependable Systems and Networks (DSN-2003)*, pp.w80–w84, San Francisco USA, June 2003.
8. Masahiro Fujita, Satoshi Komatsu, Hiroshi Saito, Kenshu Seto, Thanyapat Sakunkonchak, and Yoshihisa Kojima, "Field Modifiable Architecture with FPGAs and its Design/Verification/Debugging Methodologies," In *Proc. Hawaian International Conference on System Sciences (HICSS)*, pp.279–288, Hawai, January 2003.
9. Thanyapat Sakunkonchak and Masahiro Fujita, "Formal Verification of Synchronization Issues in SpecC Description with Automatic Abstraction," In *The 22nd IFIP International Conference on Formal Techniques for Networked and Distributed Systems (FORTE 2002)*, pp.369, Houston USA, November 2002 (Poster Presentation).
10. Hiroshi Saito, Takaya Ogawa, Thanyapat Sakunkonchak, Masahiro Fujita, and Takashi Nanya, "An Equivalence Checking Methodology for Hardware Oriented C-based Specifications," In *Proc. IEEE International High Level Design Validation and Test Workshop (HLDVT)*, pp.139–144, October 2002.
11. Thanyapat Sakunkonchak and Masahiro Fujita, "Verification of Synchronization in SpecC Description with the Use of Difference Decision Diagrams," In *Forum on specification & Design Languages (FDL'02)*, Marseille France, September 2002.
12. Thanyapat Sakunkonchak and Sawasd Tantaratana, "A High-Speed Multiplier-Free Realization of IIR Filter Using ROM's," In *Proc. of International Technical Conference & Circuits, Systems, Computers and Communications 2000 (ITC-CSCC2000)*, pp.711–714, Pusan Korea, July 2000.

13. Thanyapat Sakunkonchak and Sawasd Tantaratana, "A Pipelined Multiplier-Free Realization of IIR Filter Using ROM's and Periodically Time-Varying Structure," In *Proc. of IEEE International Symposium on Intelligent Signal Processing and Communication Systems (ISPAC'99)*, pp.597–600, Phuket Thailand, December 1999.

Local Conference Publications

1. Takeshi Matsumoto, Thanyapat Sakunkonchak, Hiroshi Saito, Satoshi Komatsu and Masahiro Fujita, "An Equivalence Checking Method for System-Level Designs Under Different Schedulings Applying Sequentialization with ILP Solvers," In *DA Symposium 2006*, pp.157–162, Hamamatsu Japan, July 2006.
2. Thanyapat Sakunkonchak, Satoshi Komatsu and Masahiro Fujita, "A Framework on Synchronization Verification in System-Level Design," In *IEICE Technical Research Report on VLSI Design Technology (VLD2005)*, Vol.104, No.708, pp.71–76, Okinawa Japan, March 2005.
3. Thanyapat Sakunkonchak and Masahiro Fujita, "Verification of Synchronization in SpecC Descriptions Using Difference Decision Diagram," In *DA Symposium 2002*, pp.137–142, Hamamatsu Japan, July 2002.
4. Thanyapat Sakunkonchak and Sawasd Tantaratana, "Implementation of ROM-Based Multiplier-Free Realization of IIR Filters," In *The 22nd Annual National Conference on Electronics, High Performance Computing, Telecommunication and Information (ECTI-22)*, Bangkok, Thailand, June, 2001.
5. Thanyapat Sakunkonchak and Sawasd Tantaratana, "A High-Speed Multiplier-Free Realization of IIR Filter Using ROM'S," In *NECTEC (Thailand) Technical Journal*, Vol.II, No.7, March-June, 2000.